AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): In a method of etching a surface of a wafer with a microscopic roughness to prepare the wafer surface for receiving a deposition of a material on the wafer surface, the steps of

removing a thin layer from the surface of the wafer to eliminate any impurities from the surface of the wafer, and

thereafter creating the microscopic roughness on the surface of the wafer to receive a deposition of the material on the surface <u>by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer</u>.

Claim 2 (cancelled)

Claim 3 (original): In a method as set forth in claim 2 wherein

the inert gas is argon.

Claim 4 (previously presented): In a method as set forth in claim 1 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on the surface of the wafer.

Claim 5 (previously presented): In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

thereafter depositing a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer, and

thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer.

Claim 6 (previously presented): In a method as set forth in claim 4 wherein

a microscopic roughness is produced on the surface of the wafer after the thin layer of the wafer has been removed from the surface of the wafer and wherein

the chromium layer is thereafter deposited on the microscopically rough surface of the wafer and wherein

a low rate of flow of an inert gas is provided on the wafer layer when the chromium layer is deposited on the surface of the wafer thereby to minimize the presence of the inert gas in the chromium layer.

Claim 7 (previously presented): In a method as set forth in claim 5 wherein

a waferland is disposed in an abutting relationship with the wafer and wherein

a layer of chromium is deposited on the surface of the waferland before etching the surface of the wafer.

Claim 8 (original): In a method as set forth in claim 5 wherein

the chromium layer is deposited on the surface of the wafer to produce an intrinsic tensile stress in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer with an RF bias power to produce an intrinsic compressive stress in the nickel vanadium layer.

Claim 9 (previously presented): In a method as set forth in claim 5 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer to produce an intrinsic tensile stress with a low stress value in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer to produce a low intrinsic compressive stress with a value to neutralize the low intrinsic tensile stress in the chromium layer.

Claim 10 (original): In a method as set forth in claim 7 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value and wherein

the layer of the nickel vanadium is deposited on the surface of the chromium in an intrinsic compressive stress with a low stress value substantially neutralizing the low stress value of the intrinsic tensile stress of the chromium layer.

Claim 11 (previously presented): In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer, and

depositing a chromium layer with a low intrinsic tensile stress on the surface of the wafer after the removal of the [impurities] thin layer from the surface of the wafer.

Claim 12 (previously presented): In a method as set forth in claim 11 wherein

the surface of the wafer is provided with a microscopic roughness after the thin layer has been removed from the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value.

Claim 13 (previously presented): In a method as set forth in claim 11 wherein

the chromium layer is deposited on the surface of the wafer in a magnetron with no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

Claim 14 (previously presented): In a method as set forth in claim 11 wherein

a chamber is provided in which to perform the recited steps and wherein molecules of an inert gas flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 15 (previously presented): In a method as set forth in claim 12 wherein

a chamber is provided in which to perform the recited steps and wherein

a waferland is disposed in the chamber to support the wafer and wherein a layer of chromium is deposited on the waferland before the chromium layer is deposited on the surface of the wafer.

Claim 16 (previously presented): In a method as set forth in claim 11 wherein

a waferland and a chamber are provided and the wafer and the waferland are disposed in the chamber and wherein

the chromium layer is deposited on the surface of the wafer in the chamber with no RF bias on the waferland in the chamber and with a low flow rate of molecules of an inert gas in the chamber,

the inert gas is argon and the flow rate of the molecules of the inert gas in the chamber is in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 17 (previously presented): In a method of providing for an attachment of an electrical component or sub-assembly to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

depositing a layer of chromium on the surface of the wafer with a low intrinsic tensile stress, and

depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

Claim 18 (previously presented): In a method as set forth in claim 17 wherein

a layer of metal selected from the group consisting of gold, silver and copper is deposited on the surface of the layer of nickel vanadium and wherein

the nickel vanadium layer has a low intrinsic compressive stress to neutralize the low intrinsic tensile stress in the chromium layer and any stress in the metal layer selected from the group consisting of gold, silver and copper.

Claim 19 (original): In a method as set forth in claim 18 wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

Claim 20. (Amended) In a method as set forth in claim 18 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland before the thin layer is removed from the surface of the wafer and wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

Claim 21 (previously presented): In a method as set forth in claim 20 wherein

a lens shield is disposed in a spaced relationship to the waferland and the lens shield is grounded and wherein

the RF bias power for the deposition of the layer of nickel vanadium is provided between the waferland and the grounded lens shield.

Claim 22 (previously presented): In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

thereafter providing the surface of the wafer with a microscopic roughness,

thereafter depositing a layer of chromium on the microscopically rough surface of the wafer with a low intrinsic tensile stress, and

thereafter depositing a layer of nickel vanadium on the surface of the wafer with a low intrinsic compressive stress.

Claim 23 (previously presented): In a method as set forth in claim 21 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

a component ~~or sub-assembly~~ is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 24 (original): In a method as set forth in claim 23 wherein

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 25 (original): In a method as set forth in claim 22 wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of the flow of an inert gas.

Claim 26 (original): In a method as set forth in claim 24 wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 27 (original): In a method as set forth in claim 2[[4]][[1]] wherein

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias and wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 28 (previously presented): In a method as set forth in claim 27 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

the component ~~or sub-assembly~~ is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 29 (previously presented): In a method of providing a deposition on a surface of a wafer, the steps of:

removing a thin layer from the surface of the wafer to eliminate impurities from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

depositing a chromium layer with a low intrinsic tensile stress on the microscopically rough surface of the wafer.

Claim 30 (original): In a method as set forth in claim 29 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber with no RF bias on the wafer, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 31 (original): In a method as set forth in claim ~~29~~ [[30]] wherein

the inert gas is argon.

Claim 32 (previously presented): In a method as set forth in claim 30 wherein

the microscopic roughness is produced on the surface of the wafer by providing the molecules of the inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 33 (previously presented): In a method as set forth in claim 29 wherein

no RF bias is provided when the chromium layer is deposited on the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent the inert gas from being entrapped in the chromium layer and wherein

the inert gas is argon.

Claim 34 (original): In a method as set forth in 31 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland, before etching the wafer surface, to prevent the layer of chromium deposited on the wafer from being contaminated by the material from the waferland.

Claim 35 (previously presented): In a method of preparing a wafer surface for receiving an electronic component, the steps of:

removing a thin layer from the surface of the wafer,

thereafter creating a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer, and

thereafter depositing a chromium layer on the microscopically rough surface of the wafer in a chamber in which a minimal amount of an inert gas is passed through the chamber during the deposition to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 36 (original): In a method as set forth in claim 35 wherein

no wafer bias is produced on the wafer when the chromium layer is deposited on the surface of the wafer.

Claim 37 (previously presented): In a method as set forth in claim 35 wherein

the chromium layer is deposited on the surface of the wafer under tension with a low amount of stress.

Claim 38 (previously presented): In a method as set forth in claim 36 wherein

the chromium layer is deposited on the surface of the wafer with a low amount of intrinsic tensile stress.

Claim 39 (previously presented): In a method of providing a deposition on a surface of a wafer for receiving an electronic component on the wafer surface, the steps of:

removing a thin layer from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

atomically bonding a chromium layer to the microscopically rough surface on the wafer.

Claim 40 (original): In a method as set forth in claim 39 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 41 (previously presented): In a method as set forth in claim 39, the step of:

providing a low intrinsic tensile stress in the chromium layer.

Claim 42 (original): In a method as set forth in claim 39 wherein

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 43 (original): In a method as set forth in claim 40 wherein

providing an intrinsic tensile stress with a low value in the chromium layer

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 44 (previously presented): In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress in the chromium layer.

Claim 45 (previously presented): In a combination as set forth in claim 44 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress <u>at a rate of flow of an inert gas in the order of 3-5 SCCM</u>.

Claim 46 (original): In a combination as set forth in claim 44 wherein

the microscopic roughness is provided on the surface of the wafer by ions of an inert gas with an insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 47 (original): In a combination as set forth in claim 44 wherein

an atomic bonding is produced between the chromium in the chromium layer and the microscopically rough surface of the wafer.

Claim 48 (previously presented): In combination for performing electrical functions,

a wafer,

a chromium layer deposited on the wafer with a low intrinsic tensile stress, and

a layer of nickel vanadium deposited on the chromium layer in firmly adhered relationship to the chromium layer with a low intrinsic compressive stress.

Claim 49 (previously presented): In a combination as set forth in claim 48,

the chromium layer being under the low intrinsic tensile stress and the nickel vanadium layer being under the low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

Claim 50 (previously presented): In a combination as set forth in claim 48,

the chromium in the chromium layer having the low intrinsic tensile stress for bonding to the microscopically rough wafer surface,

the chromium in the chromium layer having an atomic bonding with the microscopically rough surface on the wafer.

Claim 51 (previously presented): In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a chromium layer deposited on the microscopically rough surface of the wafer and atomically bonded to the microscopically rough wafer surface.

Claim 52 (previously presented): In a combination as set forth in claim 51,

the chromium layer having a low intrinsic tensile stress for bonding to the microscopically rough wafer surface.

Claim 53 (previously presented): In combination for performing electrical functions,

a wafer having a clean surface,

a chromium layer disposed on the clean surface of the wafer with an intrinsic tensile stress, and

a nickel vanadium layer deposited on the chromium layer with a low intrinsic compressive stress.

Claim 54 (previously presented): In a combination as set forth in claim 53 wherein

the low intrinsic compressive stress of the nickel vanadium layer substantially neutralizes the low intrinsic tensile stress of the chromium layer.

Claim 55 (original): In a combination as set forth in claim 53 wherein

the clean surface of the wafer has a microscopic roughness and wherein

the chromium in the chromium layer is atomically bonded to the microscopically rough surface of the wafer.

Claim 56 (previously presented): In a combination as set forth in claim 52,

a layer of a metal selected from the group consisting of copper, gold and silver and disposed on the nickel vanadium layer with a low intrinsic tensile stress.

Claim 57 (previously presented): In a combination as set forth in claim 53 wherein

a layer of a metal selected from the group consisting of copper, gold and silver is deposited on the nickel vanadium layer and wherein

the nickel vanadium layer substantially neutralizes any intrinsic stress in the metal layer selected from the group consisting of copper, gold and silver.

Claim 58 (original): In a combination as set forth in claim 53 wherein

an electrical component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 59 (previously presented): In a method of etching a surface of a wafer with a microscopic roughness, the steps of:

providing a flow of an inert gas in the order of forty (40) to fifty (50) standard cubic centimeters per minute through a chamber containing the wafer to etch a microscopic layer of material with impurities from the surface of the wafer and provide an atomic roughness to the wafer surface,

thereafter providing a flow of an inert gas through the chamber at a flow rate of approximately forty (40) to fifty (50) standard cubic centimeters per minute and a power in the order of six hundred watts (600 W) to twelve hundred watts (1200 W) to clean the surface of the wafer and increase the roughness of the wafer surface,

disposing the wafer on a waferland, and

then providing a flow of an inert gas at a rate through the chamber at a low power in the order of fifty watts (50 W) to one hundred watts (100 W) to provide the surface of the wafer with the microscopic roughness.

Claim 60 (original): In a method as set forth in claim 59 wherein

the power applied in the chamber to etch the surface of the wafer is in the order of 600-1200 watts.

Claim 61 (original): In a method as set forth in claim 59 wherein

a layer of chromium is deposited on the microscopically rough surface of the wafer without any RF bias and at a low flow rate of the inert gas.

Claim 62 (original): In a method as set forth in claim 59 wherein

a layer of nickel vanadium is deposited on the surface of the chromium layer with an RF bias power of approximately 300 watts and with a flow rate of argon of approximately 5 sccm.

Claim 63 (original): In a method as set forth in claim 60 wherein

a layer of chromium is deposited on the surface of the waferland before the surface of the wafer is etched.

Claim 64 (original): In a method as set forth in claim 60 wherein

the nickel vanadium layer is deposited on the chromium layer with a power of approximately six thousand watts (6000 W), with a flow rate of argon of approximately five (5) sccm and with RF power of approximately three hundred (300) watts.

Claim 65 (previously presented): In a method as set forth in claim 29 wherein

the chromium layer is deposited with a low intrinsic tensile stress on the microscopically rough surface by providing the layer with no RF bias.

Claim 66 (previously presented): In a method as set forth in claim 29 wherein

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 67 (previously presented): In a method as set forth in claim [[2]] [[1]] wherein

the inert gas is argon and wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on a the surface of the wafer.

Claim 68 (previously presented): In a method as set forth in claim 22 wherein

the microscopic roughness on the surface of the layer is created by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a coefficient energy to create the microscopic roughness on the surface of the wafer.

Claim 69 (previously presented): In a method as set forth in claim 39 wherein

the microscopic roughness is created on the surface of the wafer by

providing ions of an inert gas on the surface of the wafer with an

insufficient energy to etch the surface of the wafer but a sufficient energy to create the microscopic roughness on the surface of the wafer.